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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,393	CHEN ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/22/03, 02/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is a first Office action on the merits of Application Serial No. 10/600,393. Currently, claims 1-33 are pending.

Information Disclosure Statement

2. The Gonzalez et al. patent (US 6,294,421) cited in the information disclosure statement filed on 12 February 2004 has been withdrawn. Therefore, the patent has not been considered.

Specification

3. The specification is objected to as failing to provide support for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Claim 5 recites the limitation "wherein said first insulator layer is a silicon nitride layer, comprised with said first insulator thickness between about 30 to 80 Angstroms." While the specification provides support for the first insulator layer of silicon nitride having a thickness between 5 and 30 angstroms, the specification does not provide support for the first insulator layer of silicon nitride having a thickness between 30 and 80 angstroms, as recited in claim 5. The specification expressly states that the thickness of the first insulator layer is between 5 and 30 angstroms (page 5, line 20 - page 6, line 3). Correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. *Claims 3 and 4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.*

The phrase "said first pre-clean procedure" recited in claims 3 and 4 lacks antecedent basis. While claim 1 - from which claims 3 and 4 depend - recites, "performing a pre-clean procedure," the claim does not recite "a first pre-clean procedure."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. *Claims 1, 5, 8, 11, 16, 17, 19, 20, 25, 27, and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Gonzalez et al. (US 6,383,861 B1).*

The Gonzalez et al. patent (Gonzalez) discloses a method of forming multiple gate insulator layers on a semiconductor substrate (figs. 1-9 and accompanying text). With respect to claim 1, the method comprises the steps of: forming a first insulator layer 26 over a silicon containing semiconductor

substrate 12 (fig. 3 and col. 4, lines 28-40);[1] removing the first insulator layer 26 from a second portion 20 of the substrate, resulting in a first gate insulator layer having a first insulator thickness, located on a first portion 22 of the substrate (fig. 5 and col. 5, lines 11-14); performing a pre-clean procedure, wherein the pre-clean procedure can remove a native oxide from the substrate (fig. 6 and col. 5, lines 43-63);[2,3] and selectively forming a second gate insulator layer 32, having a second insulator thickness, on the second portion of the semiconductor substrate (fig. 9 and col. 6, lines 27-35).

With respect to claim 20, the method comprises the steps of: forming a first dielectric layer 26 over a silicon containing substrate 12 (fig. 3 and col. 4,

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[1] The oxide layer 24 is optional (). Thus, in one embodiment the first insulator layer 26 is formed over the substrate 12 with an intervening oxide layer 24, and in the other embodiment the first insulator layer 26 is formed over the substrate 12 with no intervening oxide layer.

[2] *Regarding the limitation "performing a pre-clean procedure, wherein said pre-clean procedure can remove a native oxide from said semiconductor substrate" recited in claim 1.* In light of the originally filed specification, the pre-clean procedure recited in claim 1 corresponds to the second of two pre-clean procedures - the first pre-clean being performed prior to forming the first insulator layer over the substrate, and the second pre-clean procedure being performed after the step of removing the first insulator layer from a second portion of the substrate and prior to the step of selectively forming second gate insulator. Whereas the recited sequence of steps implies that the pre-clean procedure of claim 1 is performed after the step of removing the first insulator layer from a second portion of the substrate and prior to the step of selectively forming a second gate insulator layer, the recited claim language does not expressly state that the pre-clean procedure must be performed in the recited order. Thus, given the broadest possible reasonable interpretation that is consistent with the specification, the pre-clean procedure recited in claim 1 can either be performed prior to the step of forming the first insulator layer - which corresponds to the first pre-clean procedure in the specification, or it can be performed after the step of removing the first insulator layer from a second portion of the substrate and prior to the step of selectively forming second gate insulator - which corresponds to the second pre-clean procedure in the specification.

[3] *Regarding the claim language "wherein said pre-clean procedure can remove a native oxide from said semiconductor substrate" recited in claim 1.* This claim language does not recite an active step, only intended use. Thus, it is not necessary to find a step for removing a native oxide. A pre-clean procedure that *is capable* of removing a native oxide from a substrate is sufficient to meet the claim limitation.

lines 28-40); selectively removing the first dielectric layer from a second portion 20 of the substrate resulting in a first dielectric gate insulator layer, having a first insulator thickness, located on a first portion 22 of the silicon containing substrate (fig. 5 and col. 5, lines 11-14); and performing an oxidation procedure to form a second dielectric gate insulator layer, having a second insulator thickness, on the second portion of the silicon containing substrate (fig. 9 and col. 6, lines 7-35), wherein the removal rate of the second dielectric gate insulator layer is higher than the removal rate of the first dielectric layer using a prescribed etchant.[4]

The first insulator/dielectric layer 26 is a silicon nitride layer with a thickness between 30 and 80 angstroms, *as recited in claim 5* (col. 4, lines 27-32). The silicon nitride layer is formed via rapid thermal chemical vapor deposition (RPCVD), and has a thickness between 5 and 30 angstroms, *as recited in claims 8 and 25* (col. 4, lines 27-40). The silicon nitride layer 26 is removed from the second portion of the substrate using a hot phosphoric acid solution, *as recited in claims 11 and 27* (col. 5, lines 10-24).[5]

The second insulator/dielectric layer 32 is a silicon oxide layer with a thickness between 30 and 80 angstroms, *as recited in claims 16 and 30* (col. 6,

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[4] The removal rate for silicon oxide is higher than the removal rate of silicon nitride when using HF as an etchant.

[5] *Regarding the claimed language "hot phosphoric acid solution" recited in claims 16 and 30.* The specification does not explicitly define the term "hot." Thus, given the broadest possible reasonable interpretation that is consistent with the specification, the phrase "hot phosphoric acid solution" is interpreted as referring to a heated phosphoric acid solution.

lines 27-35). The silicon oxide layer 32 is formed using a thermal oxidation procedure, *as recited in claim 17* (col. 6, lines 7-35).

The silicon nitride layer 26 is annealed during formation of the silicon oxide layer 32, *as recited in claim 19* (col. 6, lines 7-35).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. *Claims 2, 3, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Wolf et al. (Lu et al. (US 6,693,047 B1).*

Whereas Gonzalez discloses performing a first pre-clean procedure, prior to the formation of the first insulator layer 26, to remove an oxide film (col. 3, line 66 - col. 4, line 6), Gonzalez does not teach that either that the first pre-clean procedure is performed in a buffered hydrofluoric (BHF) acid solution comprised of HF in ammonium fluoride, or that the first pre-clean procedure is performed in a dilute HF acid solution comprised of HF in de-ionized water.

The Lu et al. Patent (Lu) discloses a method for recycling semiconductor wafers (col. 2, lines 12-18; col. 3, lines 13-40; and col. 5, lines 26-41). The method comprises removing an oxide film using either a BHF acid solution

comprised of HF in ammonium fluoride, or a dilute HF acid solution comprised of HF in de-ionized water (col. 5, lines 26-41).

Since both Gonzalez and Lu are from the same field of endeavor, the purpose for which Lu is relied upon would have been recognized in the pertinent reference of Gonzalez by one of ordinary skill in the art at the time the invention was made.

As previously stated, Gonzalez discloses performing a first pre-clean procedure, prior to the formation of the first insulator layer 26, to remove an oxide film. According to Gonzalez, the oxide film can be removed by a variety of ways, which are known in the art (col. 4, lines 4-6). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Gonzalez in view of Lu, by performing the first pre-clean procedure using either a BHF acid solution comprised of HF in ammonium fluoride or a dilute HF acid solution comprised of HF in de-ionized water, since surface treating a semiconductor substrate with HF vapors is known - in the art - to remove an oxide film on the surface of the substrate.

7. Claims 4 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Ban et al. (US 5,336,356).

Whereas Gonzalez discloses performing a first pre-clean procedure, prior to the formation of the first insulator/dielectric layer 26, to remove an oxide film (col. 3, line 66 - col. 4, line 6), Gonzalez does not teach that the first pre-clean procedure is a dry procedure performed via use of HF vapors, as recited

in claims 4 and 22. The Ban et al. patent (Ban) discloses a surface treatment apparatus, which cleans or etches an oxide film on the surface of a semiconductor wafer (col. 1, lines 7-13 and col. 2, lines 25-34). In the surface treatment, an oxide film on the surface of a semiconductor substrate is cleaned or etched using HF vapors (col. 2, lines 41-53). Ban discloses several embodiments - for example, see the embodiment described in col. 4, line 46 - col. 6, line 10.

Since both Gonzalez and Ban are from the same field of endeavor, the purpose for which Ban is relied upon would have been recognized in the pertinent reference of Gonzalez by one of ordinary skill in the art at the time the invention was made.

As previously stated, Gonzalez discloses performing a first pre-clean procedure, prior to the formation of the first insulator/dielectric layer 26, to remove an oxide film. According to Gonzalez, the oxide film can be removed by a variety of ways, which are known in the art (col. 4, lines 4-6). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Gonzalez in view of Ban, by performing the first pre-clean procedure using HF vapors, since surface treating a semiconductor substrate with HF vapors to remove an oxide film formed thereon is known in the art.

8. *Claims 6, 7, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Mosleshi et al. (US 4,715,937).*

Whereas Gonzalez discloses that the first insulator/dielectric layer 26 is a silicon nitride layer with a thickness between 5 and 30 angstroms, Gonzalez does not teach forming the silicon nitride using a direct plasma nitridization procedure, as recited in claims 6 and 23, or using a direct thermal nitridization, as recited in claims 7 and 24. The Moslehi et al. patent (Moslehi) teaches that direct plasma nitridization and direct thermal nitridization are two known methods used to form thermal nitride (col. 1, lines 21-31).

Since both Gonzalez and Moslehi are from the same field of endeavor, the purpose for which Moslehi is relied upon would have been recognized in the pertinent reference of Gonzalez by one of ordinary skill in the art at the time the invention was made.

As a result of the continuing increase in integration density of integrated circuits, and the reduction in device and circuit geometries, ultra-thin, high quality insulators are needed for gate insulators of IGFETs, storage capacitor insulators of DRAMs, and tunnel dielectrics in nonvolatile memories (Moslehi – col. 1, lines 15-21). Thermal nitrides formed using such techniques as direct plasma nitridization and direct thermal nitridization are of the best alternatives to thermally grown silicon dioxide for these particular applications (Moslehi – col. 1, lines 21-25). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Gonzalez in view of Moslehi by forming the silicon nitride layer 26, a gate insulator layer, using a method selected from one of direct plasma nitridization and direct thermal nitridization,

as taught by Moslehi, since thermal nitrides formed using such techniques are of the best alternatives to thermally grown silicon dioxide for applications such as gate insulators.

9. *Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Lucovsky et al. ("Formation of thin film dielectrics by remote plasma-enhanced chemical-vapor deposition (remote PECVD)" Applied Surface Science, Vol. 39, Issues 1-4, October 1989, pages 33-56).*

Gonzalez does not teach that the silicon nitride layer 26 is formed using remote plasma enhanced chemical vapor deposition (RPCVD) procedures, as recited in claim 9. The Lucovsky et al. reference (Lucovsky) teaches the use of remote plasma-enhanced chemical-vapor deposition to deposit thin film dielectrics such as silicon nitride (abstract, lines 1-2).

Since both Gonzalez and Lucovsky are from the same field of endeavor, the purpose for which Lucovsky is relied upon would have been recognized in the pertinent reference of Gonzalez by one of ordinary skill in the art at the time the invention was made.

With remote plasma-enhanced chemical vapor deposition, the multiplicity of reaction pathways is restricted, the stoichiometry of the silicon nitride is controlled, and the bonded hydrogen incorporation is minimized (Lucovsky - abstract, lines 5-8). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Gonzalez in view of Lucovsky by forming the silicon nitride layer 26 using remote plasma

enhanced chemical vapor deposition, as taught by Lucovsky, since with this deposition technique, the multiplicity of reaction pathways is restricted, the stoichiometry of the silicon nitride is controlled, and the bonded hydrogen incorporation is minimized.

10. *Claims 10 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Kim et al. (US 6,391,803 B1)*

Gonzalez does not teach that the silicon nitride layer 26 is formed using atomic layer chemical vapor deposition (ALCVD) procedures, as recited in claims 10 and 26. The Kim et al. patent (Kim) teaches forming silicon nitride using atomic layer chemical vapor deposition (col. 3, lines).

Since both Gonzalez and Kim are from the same field of endeavor, the purpose for which Kim is relied upon would have been recognized in the pertinent reference of Gonzalez by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Gonzalez in view of Kim by forming the silicon nitride layer 26 using atomic layer deposition, as taught by Kim, since atomic layer deposition is an alternative to conventional chemical vapor deposition methods (col. 1, lines 13-46). Furthermore, the silicon nitride layer formed using the atomic layer deposition method taught by Kim has an HF wet etching selectivity with respect to silicon oxide (col. 3, lines 5-11).

11. *Claims 12 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Wolf et al. (Silicon Processing for the VLSI Era – Vol. 1: Process Technology).*

As discussed above with respect to claims 11 and 27, Gonzalez discloses removing the silicon nitride layer 26 from the second portion of the substrate using a hot phosphoric acid solution. Whereas Gonzalez discloses using a hot phosphoric acid solution to remove the silicon nitride layer, Gonzalez does not teach removing the silicon nitride via dry etch procedures using CF_4 or Cl_2 as an etchant. The Wolf et al. reference (Wolf) teaches removing silicon nitride via dry etch procedures, wherein CF_4 is used as an etchant (page 556 - 2nd par. lines 4-9).

Since both Gonzalez and Wolf are from the same field of endeavor, the purpose for which Wolf is relied upon would have been recognized in the pertinent reference of Gonzalez by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Gonzalez in view of Wolf, by removing the silicon nitride layer 26 via dry etch procedures using CF_4 as an etchant, since dry etching using CF_4 etches silicon nitride 2-3 times faster than silicon oxide (page 556 - 2nd par. lines 7-9). Thus, when removing the silicon nitride layer on the second portion 20 of the substrate, the silicon oxide layer 24, which protects the underlying substrate, is substantially unetched.

12. *Claims 13, 14, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez.*

Whereas Gonzalez discloses performing the second pre-clean procedure (i.e. the pre-clean procedure performed after the removal of the silicon nitride layer 26 from the second portion 20 of the substrate) using a HF acid solution (col. 5, lines 43-53), Gonzalez does not teach that the HF acid solution is a BHF acid solution comprised of HF in ammonium fluoride, as recited in claims 13 and 29, or a dilute HF acid solution comprised of HF in de-ionized water, as recited in claims 14 and 29. However, since both BHF acid solution and dilute HF acid solution are HF acid solutions, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to perform the second pre-clean procedure using one or the other.

13. *Claims 15 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Ban et al. (US 5,336,356).*

Whereas Gonzalez discloses performing a second pre-clean procedure (i.e. performing a second pre-clean after removing the first insulator/dielectric layer 26 from the second portion 20 of the substrate) remove an oxide film (col. 5, lines 43-53), Gonzalez does not teach that the second pre-clean procedure is a dry procedure performed via use of HF vapors, as recited in claims 15 and 31. The Ban et al. patent (Ban) discloses a surface treatment apparatus, which cleans or etches an oxide film on the surface of a semiconductor wafer (col. 1, lines 7-13 and col. 2, lines 25-34). In the surface treatment, an oxide film on

the surface of a semiconductor substrate is cleaned or etched using HF vapors (col. 2, lines 41-53). Ban discloses several embodiments - for example, see the embodiment described in col. 4, line 46 - col. 6, line 10.

Since both Gonzalez and Ban are from the same field of endeavor, the purpose for which Ban is relied upon would have been recognized in the to pertinent reference of Gonzalez by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Gonzalez in view of Ban, by performing the second pre-clean procedure using HF vapors, since surface treating a semiconductor substrate with HF vapors to remove an oxide film formed thereon is known in the art.

14. Claims 18 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Dobuzinsky et al. (US 5,330.935).

Whereas Gonzalez discloses forming the second gate insulator/dielectric layer 32 using thermal oxidation (col. 6, lines 7-35), Gonzalez does not teach forming the silicon oxide layer 32 via a plasma oxidation procedure in an oxygen-content ambient, as recited in claims 18 and 33. The Dobuzinsky et al. patent (Dobuzinsky) teaches forming a silicon oxide film using a low temperature plasma oxidation process (col. 6, lines 31-50).

Since both Gonzalez and Dobuzinsky are from the same field of endeavor, the purpose for which Dobuzinsky is relied upon would have been

recognized in the to pertinent reference of Gonzalez by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Gonzalez in view of Dobuzinsky, by forming the silicon oxide layer 32 using a plasma oxidation procedure, as taught by Dobuzinsky, since plasma oxidation – as compared to thermal oxidation - is a low temperature oxidation process (Dobuzinsky - col. 3, lines 24-27).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
14 September 2004

Mary Wilczewski
Primary Examiner